AP7115

150mA LOW DROPOUT LINEAR REGULATOR WITH SHUTDOWN

Features

- Wide input voltage range from 2.5V to 5.5V
- 200mV low dropout voltage at 150mA output current
- Guaranteed 150mA output current.
- Low quiescent current 50µA
- Output voltage from 1.0V to 3.5V
- ±2% output voltage accuracy
- Low temperature drift at output voltage
- High PSRR
- Fast transient response
- Current limit protection
- Short circuit protection
- Thermal shutdown protection
- SOT25: Available in "Green" Molding Compound (No Br, Sb)
- Lead Free Finish/RoHS Compliant (Note 1)

General Description

The AP7115 is a 150mA, fixed output voltage, low dropout linear regulator. The device includes pass element, error amplifier, band gap reference, current-limit and thermal shutdown circuit. The characteristics of low dropout voltage and low quiescent current make it suitable for use in battery powered devices. The typical quiescent current is approximately 50µA. Several fixed output voltages are available from 1.0V to 3.5V. Additional protection is provided with built-in current-limit and thermal-shutdown functions.

Applications

- Wireless Communication
- GSM/GPRS Cellular Phones
- Handheld Mobile Devices
- Battery Powered Devices
- CD-ROM, DVD, and LAN Cards
- PC and Notebook Peripherals

Ordering Information

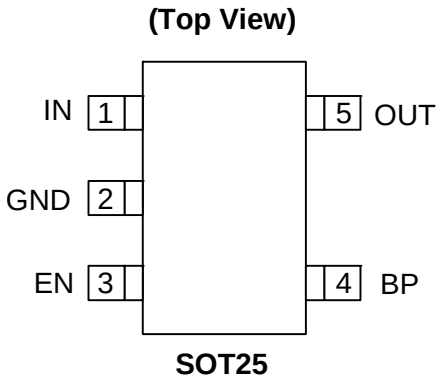
AP7115 - XX W G - 7

Output voltage	Package	Lead Free	Packing
10 : 1.0V 12 : 1.2V 15 : 1.5V 18 : 1.8V 25 : 2.5V 28 : 2.8V 29 : 2.85V 30 : 3.0V 33 : 3.3V 35 : 3.5V	W : SOT25	G : Green	7 : Tape & Reel

Device	Package Code	Packaging (Note 2)	7" Tape and Reel	
			Quantity	Part Number Suffix
AP7115-XXWG-7	W	SOT25	3000/Tape & Reel	AP7115-XXWG-7

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied, see *EU Directive 2002/95/EC Annex Notes.*
2. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

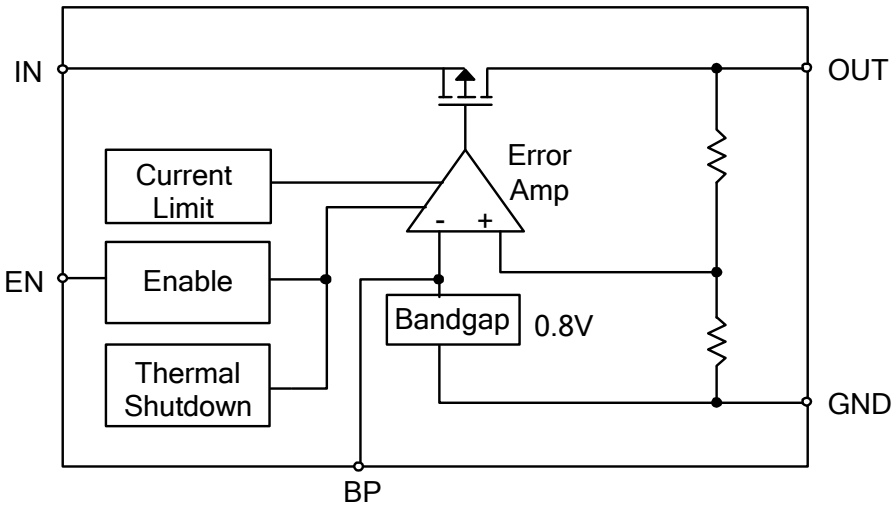
Pin Assignments



Pin Descriptions

Name	Pin NO.	Description
IN	1	Voltage Input
GND	2	Ground
EN	3	Chip Enable Control
BP	4	Band-Gap Bypass
OUT	5	Voltage Output

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
ESD HBM	Human Body Model ESD Protection	3.5	KV
ESD MM	Machine Model ESD Protection	400	V
V_{IN}	Input Voltage	-0.3~5.5	V
V_{CE}	CE Pin Voltage	-0.3~5.5	V
V_{OUT}	Output Voltage	-0.3~V_{in}+0.3	V
V_{BP}	Band Gap Bypass Pin Voltage	-0.3~5.5	V
P_D	Power Dissipation	500	mW
T_J	Operating Junction Temperature Range	-40 to +125	^oC
T_{ST}	Storage Temperature Range	-65 to +150	^oC

Recommended Operating Conditions

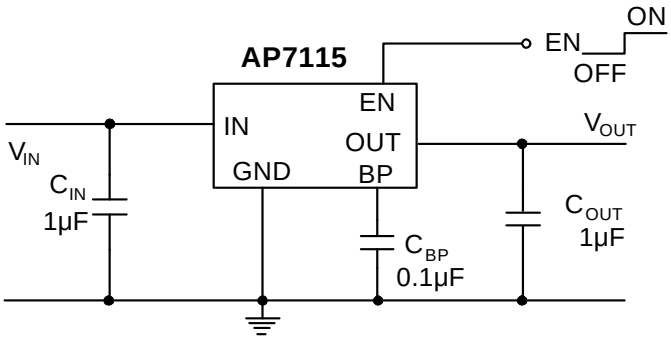
Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage	2.5	5.5	V
I_{OUT}	Output Current	-	150	mA
T_A	Operating Ambient Temperature	-40	85	^oC

Electrical Characteristics (V_{CC} = 3.3V, I_L = 30mA, C_{IN} = 1µF, C_{OUT} = 1µF, T_A = 25°C)

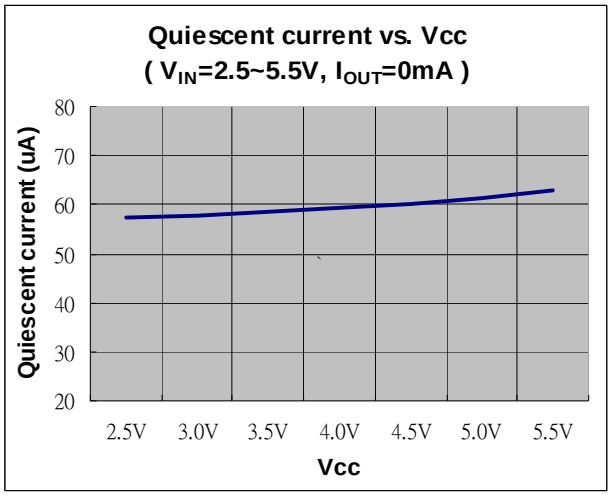
Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
System Supply Input						
V_{IN}	Operating input voltage	I_L = 0 ~ 150mA	2.5		5.5	V
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Accuracy	V_{IN} = V_{OUT} + 1V where 1mA ≤ I_{OUT} ≤ 50mA	-2		2	%
V_{DO}	Dropout Voltage	I_L = 150mA		200	300	mV
I_{OUT}	Output Current	V_{IN} - V_{OUT} = 1V	150			mA
I_Q	Quiescent Current	V_{IN} = V_{OUT} + 1V where I_{OUT} = 0 and V_{CE} = V_{IN}		50	80	µA
$I_{shutdown}$	Shutdown Current	V_{IN} = V_{OUT} + 1V where I_{OUT} = 0 and V_{CE} = 0		0.1	1	µA
PSRR	Power Supply Rejection Ratio	I_{OUT} = 30mA, f = 1kHz		70		dB
I_{limit}	Current Limit		200	250		mA
Thermal Management						
$T_{shutdown}$	Thermal Shutdown			150		°C
Reference Voltage						
$\Delta V_{REF}/\Delta T$	Tempco of Bandgap Reference			30	50	ppm/°C
$\Delta V_{OUT}/\Delta T$	Tempco of Output Voltage	I_{OUT} = 30mA, -40℃ ≤ T ≤ 85℃		50	100	ppm/°C
Control and Protection						
$V_{IH,CE}$			2.0			V
$V_{IL,CE}$					0.7	V
I_{CE}	CE Pin Leakage Current	V_{CE} = V_{IN} @V_{IN} = 5.0V and V_{SS} = 0V		0.01	0.1	µA
		V_{CE} = V_{SS} @V_{IN} = 5.0V and V_{SS} = 0V		0.01	0.1	µA
Regulation						
$\Delta V_O/\Delta V_{IN}$	Line Regulation	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V where V_{OUT} >2.0V, I_{OUT} = 30mA		0.02	0.1	%/V
ΔV_{LOAD}	Load Regulation	1mA ≤ I_L ≤ 150mA where V_{IN} = V_{OUT} + 1V		0.003	0.006	%/mA
Noise						
e_n	Output Noise	BW = 10Hz ~ 100kHz		50		μV_{rms}
Thermal Resistance						
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOT25 (Note 3)	-	200	-	°C/W
θ_{JC}	Thermal Resistance Junction-to-Case	SOT25 (Note 3)	-	52	-	°C/W

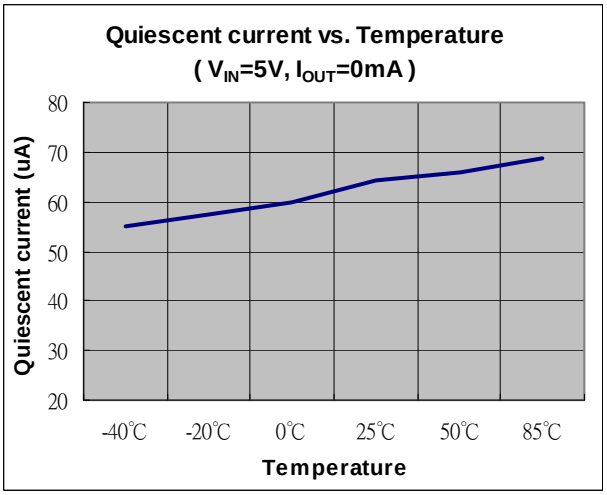
Notes: 3. Test condition for SOT25: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

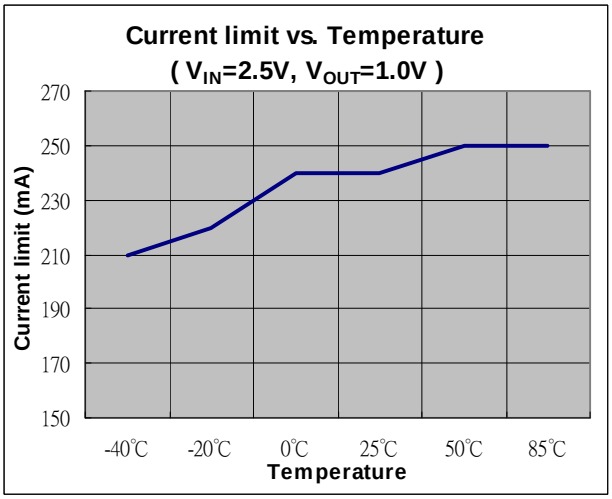
Typical Application Circuit

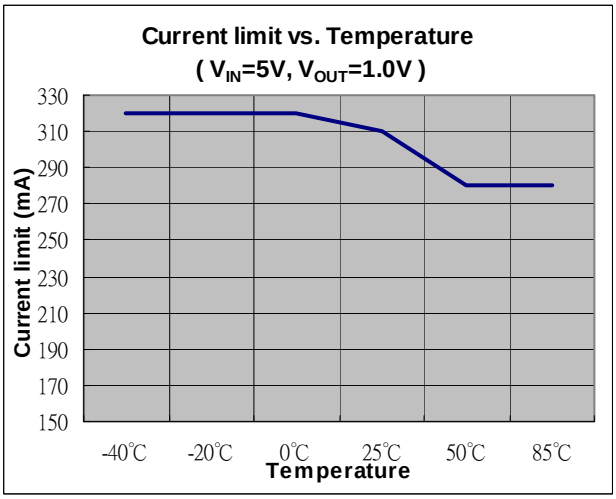


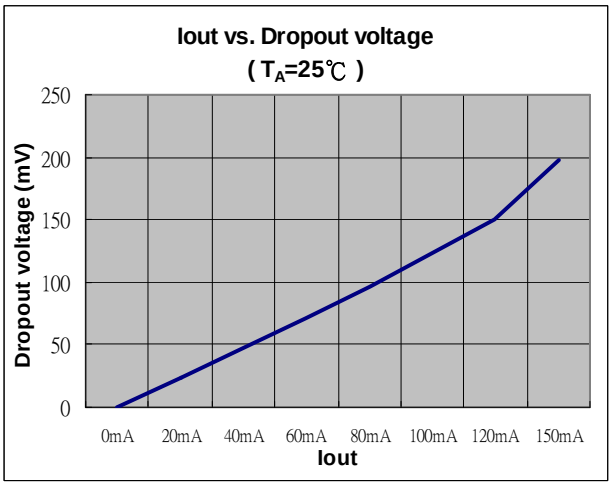
Typical Operating Characteristics

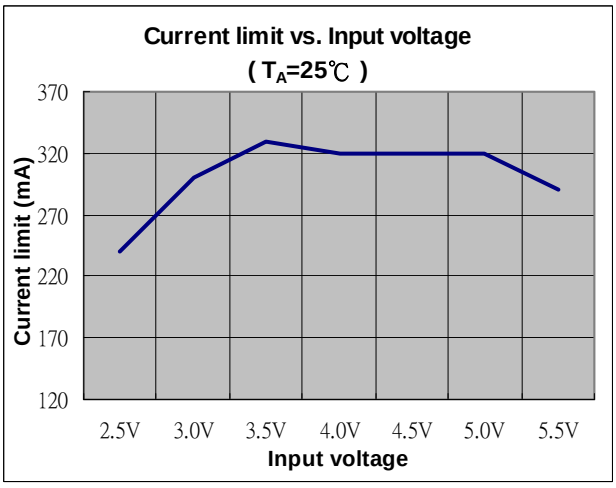




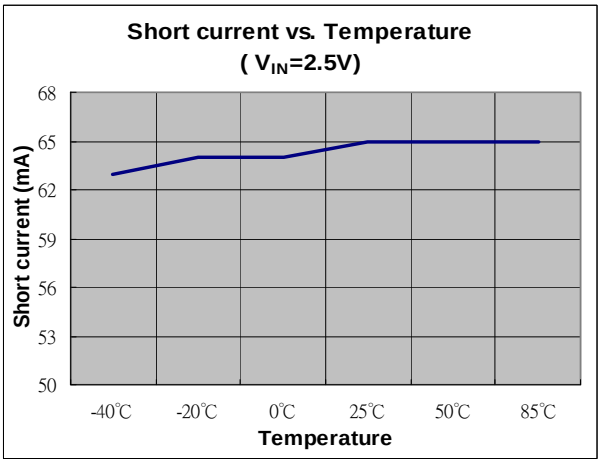


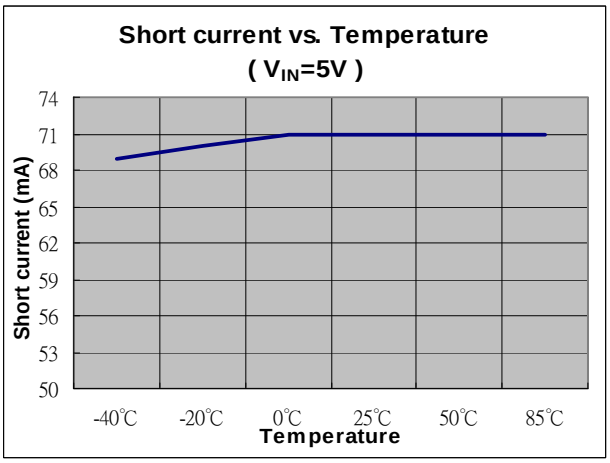


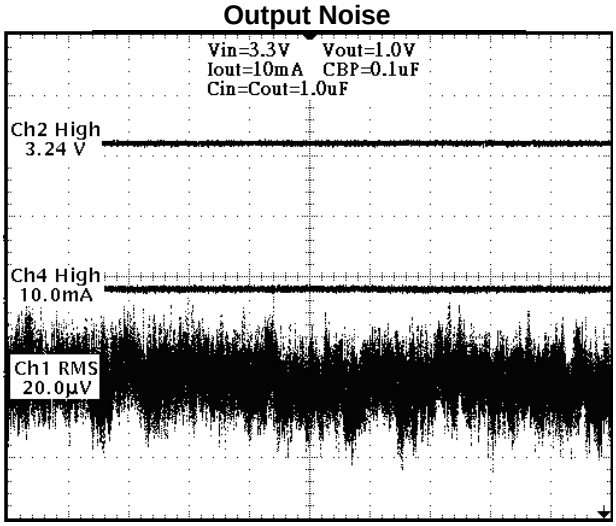


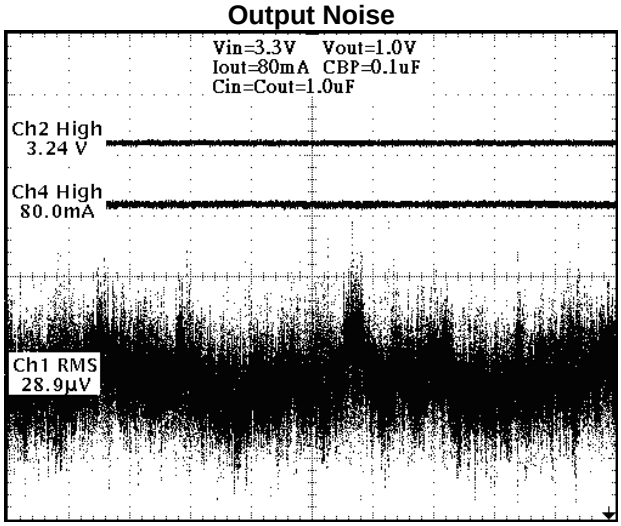


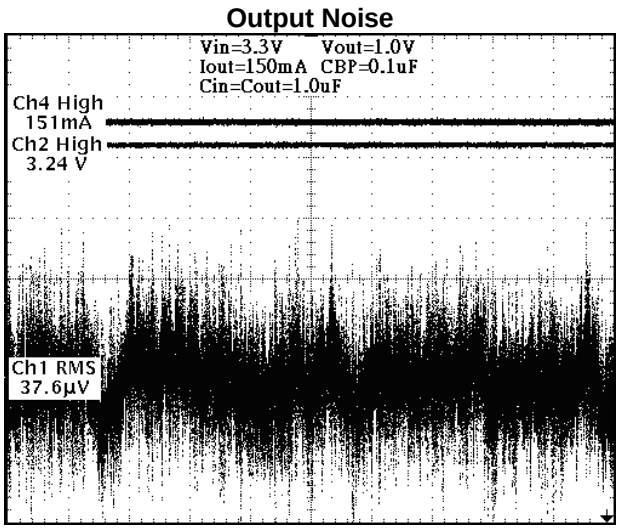
Typical Operating Characteristics (Continued)





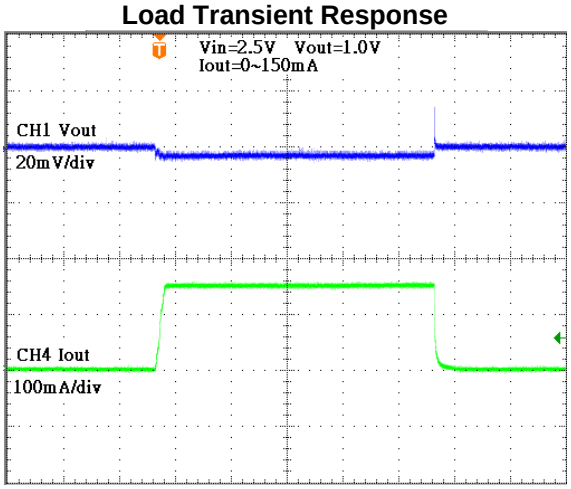




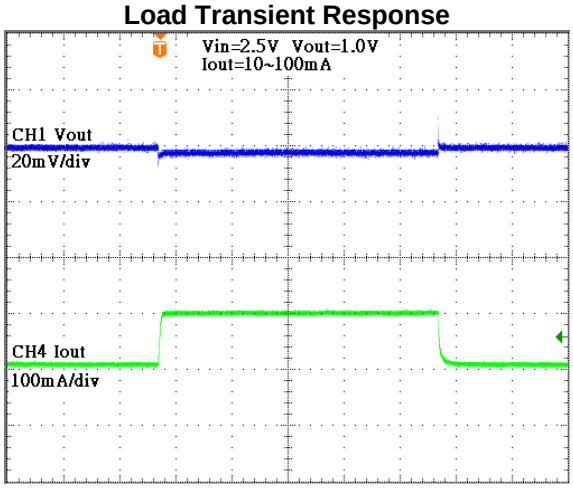


Typical Operating Characteristics (Continued)

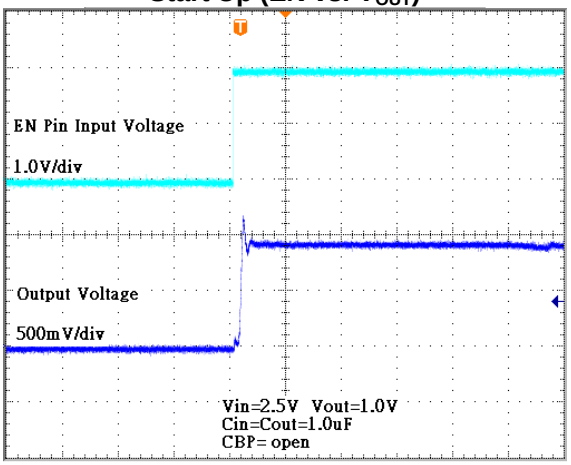
Load Transient Response



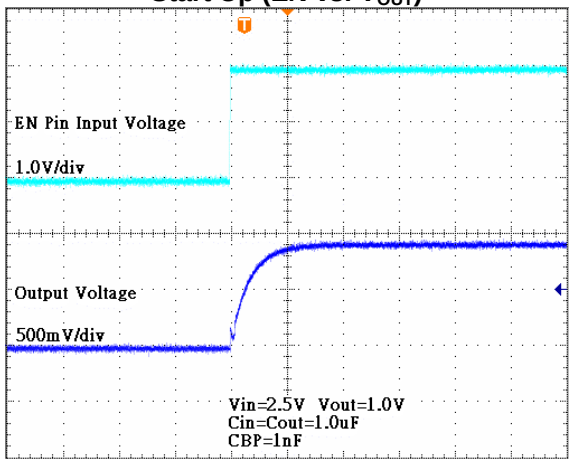
Load Transient Response



Start Up (EN vs. V_{OUT})



Start Up (EN vs. V_{OUT})



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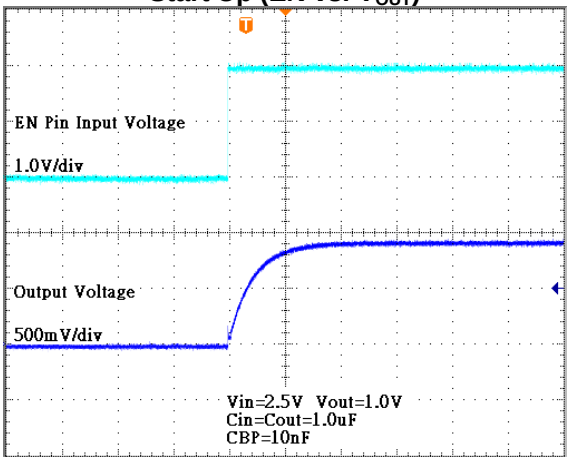
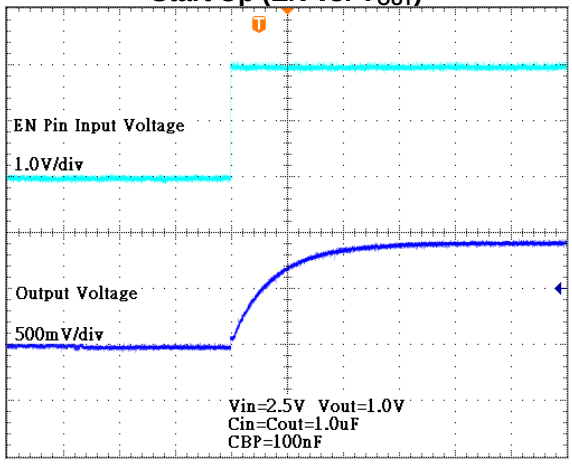


Start Up (EN vs. V_{OUT})



Application Note

■ **Input Capacitor**

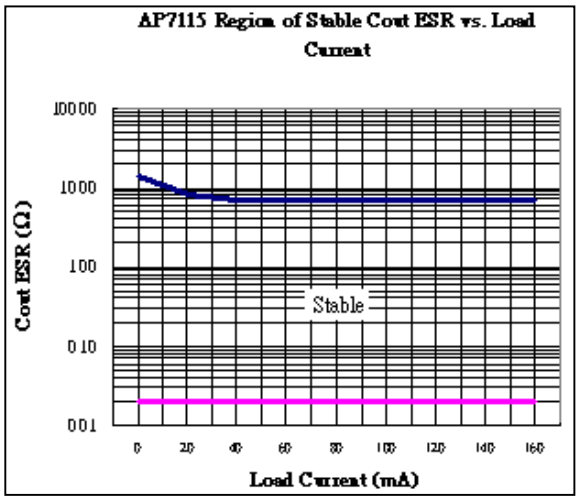
An 1uF input capacitor is required between the AP7115 input pin and GND.

There are no requirements for the ESR on input capacitor, but tolerance and temperature coefficient must be considered.

■ **Output Capacitor**

The AP7115 can work with very small ceramic output capacitors (1uF or greater). Higher capacitance values help to improve transient. The output capacitor's ESR is critical because it from a zero to provide phase lead which is required for loop stability.

Figure below is Cout ESR vs. Load Current.



■ **Band-Gap Bypass Capacitor**

0.1uF bypass capacitor Between BP pin and GND can reduces output voltage noise.

■ **Shutdown Input Operation**

The AP7115 is shutdown by pulling the EN pin low, and turned on by driving the input high. If the shutdown feature is not required, the EN pin should be tied to VIN to keep the regulator on at all times.

■ **Dropout Voltage**

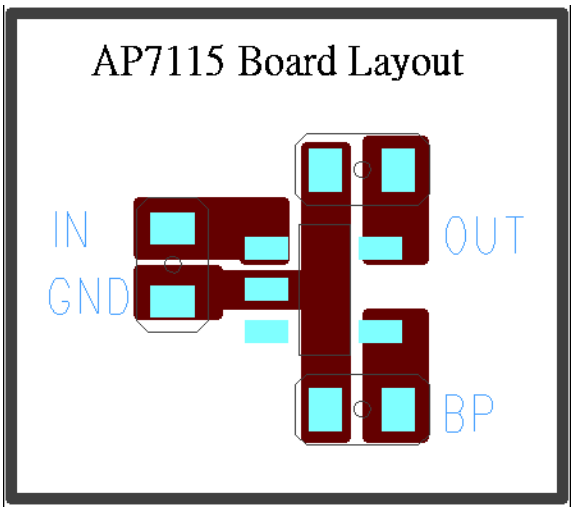
$V_{DROPOUT} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{OUT}$

■ **Current Limit**

The AP7115 monitors and controls the PMOS' gate voltage, limiting the output current to 250mA(typ.). The output can be shorted to ground for an indefinite period of time without damaging the part.

■ **PCB Layout**

Optimum performance can only be achieved when the device is mounted on a PC board according to the diagram below:



■ **Thermal Considerations**

Thermal Shutdown Protection limits power dissipation in AP7115. When the operation junction temperature exceeds 155°C, the Over Temperature Protection circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 30°C. For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

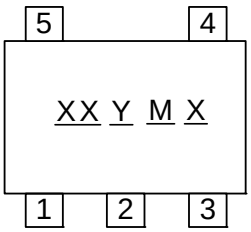
The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

Marking Information

(Top View)

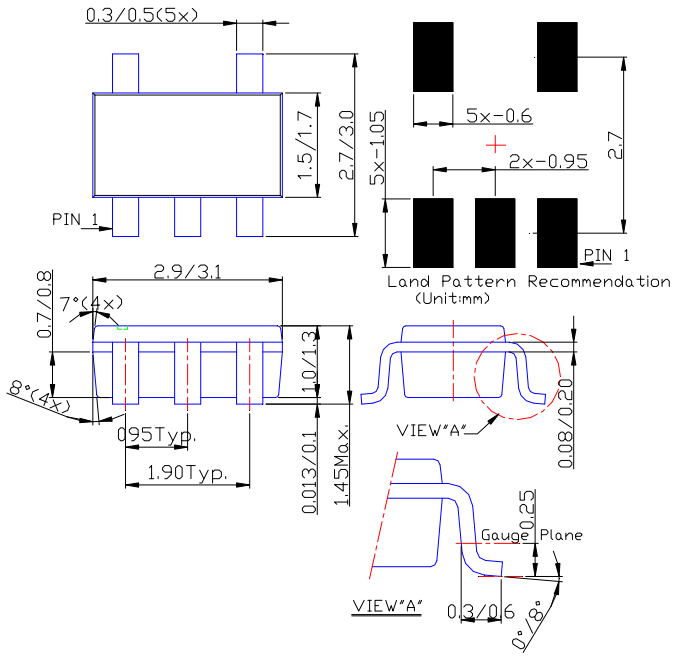


XX : Internal code
Y : Year 0~9
M : Month A~L
X : G : Green

SOT 25

Part Number	Package	Identification Code
AP7115-10W	SOT25	FO
AP7115-12W	SOT25	FP
AP7115-15W	SOT25	FQ
AP7115-18W	SOT25	FR
AP7115-25W	SOT25	FS
AP7115-28W	SOT25	FT
AP7115-29W	SOT25	FU
AP7115-30W	SOT25	FV
AP7115-33W	SOT25	FW
AP7115-35W	SOT25	FX

Package Information (All Dimensions in mm)



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